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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,495	SHAVIT ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-110* is/are pending in the application.

4a) Of the above claim(s) *34-51 and 67-106* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33,52-66 and 107-110* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/19/05, 1/3/06*. 1/31/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-33, 52-66, and 107-110 are pending in the Application.

Claims 34-51, and 67-106 are withdrawn in response to Examiner's restriction requirement.

Claims 107-110 are new

Claims 1-33, 52-66, and 107-110 are rejected.

Election/Restrictions

2. Applicant's election without traverse of Group I, and subsequent withdrawal of claims from groups II-IV in the reply filed on 28 July 2006 is acknowledged.

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-33, and 52-66, drawn to a method and computer program product for single-swap synchronization with snapshot facility, classified in class 711, subclasses 141 and 162.

II. Claims 34-39, and 43-51, drawn to a method for multiple target non-blocking synchronization of instruction sequencing, classified in class 711, subclass 141, with mandatory search in class 712, subclass 216.

III. Claims 40-42, 67-82, and 103-106, drawn to a method and apparatus for load-linked and store-conditional sequence emulation, classified in class 712, subclass 216, with mandatory search in class 711, subclass 147.

IV. Claims 83-102, drawn a method and computer program product for a non-blocking load-linked and store-conditional sequencing including via a compare and swap based implementation, classified in class 711, subclasses 141 and 163, with mandatory search in class 712, subclass 208.

4. The inventions are distinct, each from the other because of the following reasons: Inventions I, II, III and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility from inventions II-IV such as use in a system employing snapshotting of applicant values in order to synchronize targeted locations for the purpose of ensuring that locations remain the unchanged following the snapshot. Invention II has separate utility from inventions I, and III-IV such as use in a system employing instruction sequencing among multiple locations in a multiprocessor system. Invention III has separate utility from inventions I-II, IV such as use in a system for instruction emulation (i.e. load-linked and store-conditional). Finally, invention IV has separate utility from inventions I-III such as use in a system for load-linked and store-conditional sequencing including via a compare and swap operation.

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper. See MPEP § 806.05(d).

Information Disclosure Statement

6. The three information disclosure statements (IDS) submitted on 19 December 2005, 3 January 2006, and 31 January 2006 were fully considered by the examiner.

Drawings

7. The drawings were received on 24 September 2003. These drawings are deemed acceptable for examination.

Specification

8. The abstract of the disclosure is objected to because of the following:

All extraneous markings (i.e. "Attorney Docket ...") should be removed from the abstract.

Correction is required. See MPEP § 608.01(b).

9. The disclosure is objected to because of the following informalities:

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The computer readable

medium recited in the claims does not appear to be present in Applicant's original specification.

Appropriate correction is required.

Claim Objections

10. Claims 1-20, 22-31, 54-57, 63, and 66 are objected to because of the following informalities:

As for claim 1, the phrase "that ensure" as recited in line 7 should be changed to "ensure" for clarity.

As for claim 3, the word "target" as recited in lines 2 and 3 in this claim should be changed to "location" to properly establish antecedent basis.

As for claim 8, 20, 22, 31, 54, 63, acronyms (such as CAS) should not be used to abbreviate key phrases until they are explicitly defined previously within the claim, or in a claim to which it depends. An acceptable correction would be "compare-and-swap (CAS)".

As for claim 23, the phrase "updates state" and "verifies state" as recited in lines 2 and 3 of this claim should be changed to "updates a state" and "verifies a state" for clarity.

As for claim 66, the phrase "medium includes" as recited in line 2 of this claim should be changed to "media include" for clarity.

Claims 2-20, 24-30, 56-57 are objected to for further limiting claims 1, 23, and 55 respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

11. Claims 21-33 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. More specifically, Examiner is unable to determine which (if any) of the four statutory categories of patentable subject matter claim 21 falls into. More specifically, claim 21 appears to be a process (i.e. method for implementing a k-compare, single swap synchronization employing no more than two atomic, single-location read-modify-write synchronization), however upon review of the claims further limiting claim 21 (i.e. claim 23), Applicant recites the implementation further comprising "a update mechanism" and "a snapshot mechanism" which seems to imply the previously recited implementation is an article of manufacture, requiring some sort of mechanism or device to carry out the process recited in claim 21.

Claims 22-33 are rejected for further limiting claim 21.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1-20, 24-26, 52-66, and 107-110 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 52, and 107 recite the limitation "the application values" (in lines 3-4 of claim 1 for example). There is insufficient antecedent basis for this limitation in the claim. More specifically, multiple applications values are not previously set forth within these claims.

Claim 7, recites the limitation "the non-blocking property" in line 2 of this claim. There is insufficient antecedent basis for this limitation in the claim. More specifically, a non-blocking property is not set forth previously set forth within this claim or the claim from which it depends.

Claim 10, recites the limitation "the targeted location" in lines 4-5 of this claim. There is insufficient antecedent basis for this limitation in the claim. More specifically, a plurality of target locations are previously set forth in claim 1. Which target location is being referenced here?

Claim 20, recites the limitation "the load-linked and store-conditional sequences" in line 2 of this claim. There is insufficient antecedent basis for this limitation in the claim. More specifically, a neither load-linked nor store-conditional sequences are previously set forth within this claim or the claim from which it depends.

Claim 24, recites the limitation "the first application value" in line 3 of this claim. There is insufficient antecedent basis for this limitation in the claim. More specifically, a

first application value is not set forth previously set forth within this claim or the claim from which it depends.

Claims 2-20, 25-26, 53-66, and 108-110 are rejected for further limiting claims 1, 24, 52, and 107 respectively.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 21 and 31 are rejected under 35 U.S.C. 102(b as being anticipated by MacGregor et al. (US Patent 4,584,640), hereinafter MacGregor.

As for claim 21, MacGregor teaches an obstruction-free implementation of a k-compare, single-swap synchronization construct that, in an uncontended execution thereof, employs no more than two (2) atomic, single-location read-modify-write synchronizations (referring to Fig. 3A and 3B, Macgregor teaches performing a compare and swap operations via two single-location RWM cycles – col. 6, lines 26-52).

As for claim 31, MacGregor, teaches the single-location synchronizations are compare-and-swap (CAS) synchronizations (col. 2, lines 16-42).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1-5, 9, 11, 14-17, 23, 24, 26, 29, 30, 52, 53, 55, 57, 60-63, 66, 107-109 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacGregor (US Patent 4,584,640) as applied to claim 21 above, and in further view of Greenspan et al. (US Patent 6,128,710), hereinafter Greenspan.

As for claims 1, 23, 52 and 107, MacGregor teaches a method of providing a linearizable multi-compare, single-swap facility for concurrent software, the method comprising:

snapshotting values corresponding to targeted locations, and employing a pair of single-location synchronizations to that ensure that the values corresponding to a first targeted location remained unchanged at a linearization point of the snapshot (referring to the flow diagrams illustrated in Fig. 3A and 3B, MacGregor teaches writing first and second swap values to first and second test locations respectively during the compare-and-swap operation (i.e. snapshotting) - col. 6, lines 26-53).

Despite these teachings MacGregor fails to teach specifically the use of application values, and updating a first application value corresponding to a first

targeted location only if the application values corresponding to plural other targeted locations remain unchanged.

Greenspan however teaches a method utilizing a set of block-symbol resource-manipulation instructions for protecting the integrity of data in noncontiguous data objects of resources in a shared memory of a multiple processor computer system. More specifically, Greenspan discloses serialization control via the use of blocking symbols. A processor is capable of checking and changing the locks of a particular memory location only if the other locations remain locked (i.e. unchanged) – col. 5, lines 28-42. Additionally note that the blocking symbols themselves are stored with the data, therefore snapshotting of the data as taught by MacGregor would include snapshotting the application values;

It would have been obvious to one of ordinary skill in the art at the time of the invention for MacGregor to further include Greenspan's method of protecting the integrity of data in noncontiguous data objects into his own compare and swap method. By doing so, MacGregor could benefit by exploiting Greenspan's means of improving security and integrity of his own stored data as taught by Greenspan in col. 3, lines 32-41.

As for claims 2, 15, 30 and 61, MacGregor teaches wherein the first targeted location and at least one of the other targeted locations are non-contiguous (col. 5, lines 8-14).

As for claim 3, MacGregor teaches wherein a first one of the single target synchronizations precedes the snapshotting, and wherein a second one of the single

target synchronizations follows the snapshotting (Fig. 3B - the RMW command write occurs before the write operation).

As for claim 4, MacGregor teaches wherein the second one of the single target synchronizations effectuates the updating (Fig. 3B, col. 6, lines 26-53)

As for claim 5, MacGregor teaches wherein the single-location synchronizations retry on failure (Fig. 3A, system will retry upon bus failure).

As for claims 9, 24, and 55, MacGregor teaches displacing the first application value from the first targeted location prior to the linearization point of the snapshotting (Fig. 3B - the RMW command write occurs before the write operation).

As for claims 11, 26 and 57, MacGregor teaches wherein the displacing is performed by a load-linked sequence that employs one of the single-location synchronizations (col. 6, lines 26-52).

As for claims 14, 29 and 60, MacGregor teaches wherein any particular application value is read either from a corresponding one of the targeted locations, if encoded therein, or from an auxiliary location associated with an id, if instead, the id is encoded therein (col. 6, lines 26-52).

As for claim 16 and 63, MacGregor, teaches the single-location synchronizations are compare-and-swap (CAS) synchronizations (col. 2, lines 16-42).

As for claims 17 and 62, MacGregor the single-location synchronizations as being atomic read-modify-write synchronizations (col. 6, lines 25-35).

As for claim 53, MacGregor teaches his system as employing no more than two (2) atomic, single-location read-modify-write synchronizations (referring to Fig. 3A and

3B, Macgregor teaches performing a compare and swap operations via two single-location RWM cycles).

As for claim 66, MacGregor teaches the medium as including a disk (Fig. 1, element 26).

As for claims 108 and 109, MacGregor teaches embodying code that present a linearizable multi-compare, single swap operation executable in a computer system (referring to Fig. 3A and 3B, Macgregor teaches performing a compare and swap operations via two single-location RWM cycles).

15. Claims 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacGregor (US Patent 4,584,640) as applied to claim 21 above, and in further view of Yeh et al. (US PG Publication 2003/0105943 A1), hereinafter Yeh.

As for claims 32-33, though MacGregor teaches all the limitations of the base claim, he fails to teach wherein the single-location synchronizations are compare-and-swap (CAS) synchronizations employed to define a load-linked (LL) sequence and a store-conditional (SC) sequence, respectively. Yeh however teaches a mechanism for processing speculative LL and SC instructions in a pipelined processor employing both LL and SC operations (paragraphs 0010 through 0011, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for MacGregor to further include Yeh's mechanism for processing speculative LL and SC instructions into his own compare and swap system. By doing so, MacGregor would benefit by having a more effective means of monitoring system

addresses, while avoiding the possibility of ceasing the monitoring operation should an exception occurs as taught by Yeh in paragraph 0009, all lines.

16. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over MacGregor (US Patent 4,584,640) as applied to claim 21 above, and in further view of Bonola (Us PG Publication 2003/0065892 A1)

As for claim 22, though MacGregor teaches all the limitations of claim 21, he fails to teach employing tagged id displacement for ABA avoidance. Bonola however teaches the use of tagged ids for ABA avoidance (paragraph 0013, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for MacGregor to further include Bonola's Non-blocking FIFO array into his own system for compare and swap operations. By doing so, MacGregor would be able to further avoid deadlock situations as discussed by Bonola in paragraph 0010, all lines.

17. Claims 6-8, 20, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacGregor (US Patent 4,584,640) and Greenspan (US Patent 6,128,710) as applied to claims 1 and 52 above, and in further view of Bonola (US PG Publication 2003/0065892 A1)

As for claims 6, 7 and 20, though the combined teachings of MacGregor and Greenspan teach all the limitations of the base claims, they fail to teach employing a non-blocking property including obstruction-freedom. Bonola however teaches a concurrent non-blocking FIFO array which employs a non-blocking queue for obstruction freedom (paragraph 0026, all lines).

As for claims 8 and 54, though the combined teachings of MacGregor and Greenspan teach all the limitations of the base claims, they fail to teach the single-location synchronizations as employing tagged id displacement for ABA avoidance. Bonola however teaches the use of tagged ids for ABA avoidance (paragraph 0013, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for MacGregor to further include Bonola's Non-blocking FIFO array into his own system for compare and swap operations. By doing so, MacGregor would be able to further avoid deadlock situations as discussed by Bonola in paragraph 0010, all lines.

18. Claims 18,19, 64, 65 and 110 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacGregor (US Patent 4,584,640) and Greenspan (US Patent 6,128,710) as applied to claims 1 and 52 above, and in further view of Yeh (US PG Publication 2003/0105943 A1)

As for claims 18,19, 64, 65 and 110, though the combined teachings of MacGregor and Greenspan teach all the limitations of the base claims, they fail to teach wherein the single-location synchronizations are compare-and-swap (CAS) synchronizations employed to define a load-linked (LL) sequence and a store-conditional (SC) sequence, respectively. Yeh however teaches a mechanism for processing speculative LL and SC instructions in a pipelined processor employing both LL and SC operations (paragraphs 0010 through 0011, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for MacGregor to further include Yeh's mechanism for processing speculative

LL and SC instructions into his own compare and swap system. By doing so, MacGregor would benefit by having a more effective means of monitoring system addresses, while avoiding the possibility of ceasing the monitoring operation should an exception occurs as taught by Yeh in paragraph 0009, all lines.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CEW

Craig E Walter
Examiner
AU 2188

Mano Padmanabhan 8/31/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER